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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,253	01/02/2002	Robert C. Glenn	42390P12280	9323

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EXAMINER

WONG, LINDA

ART UNIT PAPER NUMBER

2611

DATE MAILED: 06/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/039,253

Applicant(s)

GLENN ET AL.

Examiner

Linda Wong

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 March 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,6-24,26,27 and 31-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,6-11,13,17 and 20-24 is/are rejected.
- 7) ☒ Claim(s) 12,14-16,18,19,26,27 and 31-37 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Applicant's Remarks, filed 3/9/2006, with respect to the rejection(s) of claim(s) 1,6-16,24,26-27 under Chao et al have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.
2. Applicant's arguments with respect to claims 17-23 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. **Claim 1** recites the limitation "phase control circuitry ... adjust a proportion of the amplitude contributions..." Is the limitation "proportion of the amplitude contribution" the same as the previously mentioned limitation "interpolator circuitry to proportion amplitude contributions of reference clock phases"? If so, please include antecedent basis for the limitation "proportion of the amplitude contributions".
4. **Claim 31** recites the limitation "phase control circuitry ... adjust a proportion of the amplitude contributions..." Is the limitation "proportion of the amplitude contribution" the same as the previously mentioned limitation "interpolator circuitry to proportion amplitude contributions of reference clock phases"? If so, please include antecedent basis for the limitation "proportion of the amplitude contributions".

Claim Rejections - 35 USC § 112

5. **Claim 24** is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: degenerative mesh circuitry and its relationship with the rest of the components in the phase interpolator. The examiner understands that the degenerative mesh is coupled between the first and second circuitry but it is unclear as to the relationship between the degenerative mesh and for instance, the phase control circuitry or the output circuitry or the interpolator circuitry.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1,6-11** are rejected under 35 U.S.C. 102(e) as being unpatentable by Chao et al (US Patent No.: 6380783).
- a. **Claim 1**, Chao et al discloses a interpolator circuitry using a weighted bias current to adjust the clock phases (Fig. 1, labels 18,IA,IB and Col. 5, lines 18-32), a phase control circuit (Fig. 1, label 16 and Col. 4, lines 1-7) for adjusting the phases based on a controlled signal (Fig. 1, label D<2:0> and Col. 5, lines 5-16), a degenerative mesh (Fig. 5, labels Resistor and Vcom), wherein the mesh regulates the bias current IA (Fig. 1, output from label 16) when the

inverse clk_a turns the switch on (Fig. 5, label 78) and bias current IB (Fig. 1, output from label 16) when the clk_b turns the switch on (Fig. 5, label 82) and an output circuitry for outputting a phase based on the adjusted clock phases. (Fig. 1, label 20)

- b. **Claim 6**, Chao et al suggests in Fig. 5, the degenerative mesh comprised of the resistors and Vcom as shown in Fig. 5 as providing substantially equivalent impedances between the two currents (Fig. 5, labels IA and IB) provided by the phase control circuitry (Fig. 1, labels 16 and 34 and Col. 4, 1-15).
- c. **Claims 7**, Chao et al discloses an interpolator comprising a current-steering mechanism for adjusting the current based on the bias current generated. (Fig. 5A, and Col. 5, lines 18-67 and Col. 6, lines 1-19)
- d. **Claim 8**, Chao et al discloses steering the current between two conductive paths. (Figures 5 and 5A and Col. 5, lines 18-65)
- e. **Claim 9**, Chao et al discloses an interpolator comprising a current-steering mechanism wherein the weighted bias currents adjust the clock phases. Since the bias currents are weighted and the clock phases are adjusted based on these bias currents, it would be obvious to one skilled in the art that the amplitude of the bias currents affect the adjustments of the amplitude of the clock phases. (Fig. 5A, Col. 5, lines 18-67 and Col. 6, lines 1-19)
- f. **Claim 10**, Chao et al discloses the phase control circuitry (Fig. 1, labels 16 and 34 and Col. 4, lines 1-16) coupled to the interpolator (Fig. 1, label 18) to adjust

the amplitude (Col. 4, lines 25-46 and Col. 5, lines 6-16) based on the control signals (Fig. 1, label 34).

- g. **Claim 11**, Chao et al discloses a connection between the weighted bias current and the current steering mechanism or phase interpolator (Fig. 1, labels 16 and 18) Although Chao et al does not explicitly state a conductive path coupled between the current source and current-steering mechanism, in order to produce a current to the phase interpolator, it is inherent to use a conductive path.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claims 13,17,20-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al (US Patent No.: 6380783) in view of Buchwald et al (US Patent No.: 6509773).
- a. **Claim 13**, Although Chao et al does not teach combining the first and second phases, Buchwald et al discloses combining a plurality of adjusted phases outputted. (Col. 2, lines 26-28, Fig. 9, labels 804 and 826 and Col. 15, lines 35 and 39) It would be obvious to one skilled in the art to replace the comparator found in Chao et al with the combiner found in Buchwald et al to provide

adjusted phase based on multiple changes to effectively sample high data rate signals to reduce cost, size and power dissipation.

- b. **Claim 17**, Chao et al discloses receiving a plurality of clocks with different phases (Fig. 1, labels 26,28,30,32), providing interrelated control signals (Fig. 1, label 34) associated with the first and second phase (Fig. 1, labels D<2:0> and Col. 4, lines 1-15), proportioning the phases (Fig. 18, labels 26,28,30,32,36,38,14 and 18) based on the interrelated control signals (Fig. 1, label 16, Fig. 5) Although Chao et al does not teach combining the first and second phases, Buchwald et al discloses combining a plurality of adjusted phases outputted. (Col. 2, lines 26-28, Fig. 9, labels 804 and 826 and Col. 15, lines 35 and 39) It would be obvious to one skilled in the art to replace the comparator found in Chao et al with the combiner found in Buchwald et al to provide adjusted phase based on multiple changes to effectively sample high data rate signals to reduce cost, size and power dissipation. Although Chao et al and Buchwald et al fails to discloses interrelated ramping voltage control signals, Chao et al discloses current control signals, wherein current is related to voltage and the current control signals can easily be translated to voltage control signals. It would be obvious to one skilled in the art to perform such a task based on design choice.
- c. **Claim 20**, Chao et al discloses receiving more than 1 phase of a reference clock signal (Fig. 1, labels 26,28,30 and 32), wherein the phases outputted to

the selector found in Chao et al comprises two phases that are less than 180 degrees apart. (Col. 3, lines 54-59)

- d. **Claim 21**, Chao et al discloses receiving control signals, wherein the first and second control signal (Fig. 1, labels clk_a and clk_b) are used to control, along with the bias currents, IA and IB, the increase and decrease in charge. (Col. 5, lines 18-43) Although Chao et al does not explicitly disclose adjusting the amplitude, the bias currents, IA and IB, are weighted and used to control the adjustments along with the control signals, clk_a and clk_b. It is obvious to one skilled in the art that the amplitude would be adjusted when using a weighted bias current to adjust the charge.
- e. **Claim 22**, Chao et al discloses increasing the charge, controlled by clk_a, clk_b, IA and IB, at the same rate as decreasing the charge. Although Chao et al does not explicitly disclose an increase and decrease at the same rate, in Figure 6, the charge is displayed. The amplitudes are shown to increase and decrease at the same rate. (Fig. 6 and Col. 5, lines 43-65)
- f. **Claim 23** inherits all the limitations of claim 13 but claim 13 does not recite the first and second phase are proportioned based upon the voltage of the interrelated control signals. Chao et al discloses control signals wherein the phase interpolator adjusts the phase based on the voltage of clk_a and clk_b. (Fig. 6, and Col. 5, lines 18-43)

Allowable Subject Matter

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8. **Claims 18,32-37** are objected to as being dependent upon a rejected base claim.
9. **Claim 19** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
10. **Claim 31** would be allowable if rewritten to overcome the objection(s).
11. **Claim 24** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.
12. **Claims 12,14-16,26-27** are objected as being dependent upon a rejected base claim, but would allowable if the independent claim is rewritten to overcome the 35 USC 112 rejection(s).

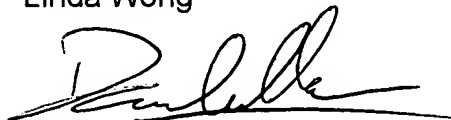
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Linda Wong



**DACHA
PRIMARY EXAMINER**